YM3802

MIDI Communication & Service Controller (MCS)

■ OUTLINE

The YM3802 is an LSI device featuring an asynchronous serial communication interface, a frequency divider that acts a communication rate generator, an interface for the cassette tape recorder, transmit/receive data buffers, timers, counters and a parallel input/output port. With this LSI a part of the MIDI data processing can be performed by hardware.

The YM3802 LSI has two output pins and three counters that synchronize with the MIDI clock and the tape SYNC can be easily realized. The MIDI clock is generated by the MIDI clock timer, the tape SYNC signal or the clock message which is contained in the received serial data. Another way of the generation of the MIDI clock is a process with the host CPU control. This LSI has the priority transmission and reception capability of the MIDI system real-time message over other messages and also can support the processing of the system exclusive message.

Each of the MIDI counters can be utilized as general-purpose timer/counter.

■ FEATURES

- Serial communication
  7- or 8-bits ..... Character
  1- or 4-bits ..... Parity bit,
  1- or 2-bits ..... Stop bit,
  Start bit error detection,
  Automatic break detection and break character generation,
  Character length, Types of parity and stop bits and communication rate are selectable for transmission and reception separately.

- Cassette tape recorder interface
  One-wave/two-wave FSK modulation,
  Automatic follow-up function for polarity and phase,
  Transfer-rate check function,
  Used for ordinary serial communication or cassette tape recorder interface in transmission and reception (separately).

- Communication rate generator
  Communication rate generation of 75 ~ 19200 bps and 31.25K bps.
  Reception is performed at the internal clock rate which is 16 times the communication rate.
  Communication rates of DC through 125K bps can be obtained by selecting the frequency of the communication rate generating clock.

- General-purpose 8-bit parallel input/output port.

- General-purpose 14-bits timer.

- 128 bytes FIFO buffer for reception and 16 bytes FIFO buffer for transmission.

- MIDI support functions
  SYNC out, CLOCK out; output of a pulse signal synchronized to the system real-time message.
  Automatic transmitting function, priority transmitting function and priority receiving function (without involving the receiving FIFO buffer) of the system real-time message.
  8- and 15-bit counters for counting the interpolated, high-accuracy signal of the MIDI clock.
  Special 14-bit timer for determining MIDI clock generation timing. Detecting function of the MIDI clock from the received serial data.
  Tape SYNC function.
  Automatic output of the tape SYNC signal
  Active sense function
  ID code check function for the system exclusive message.

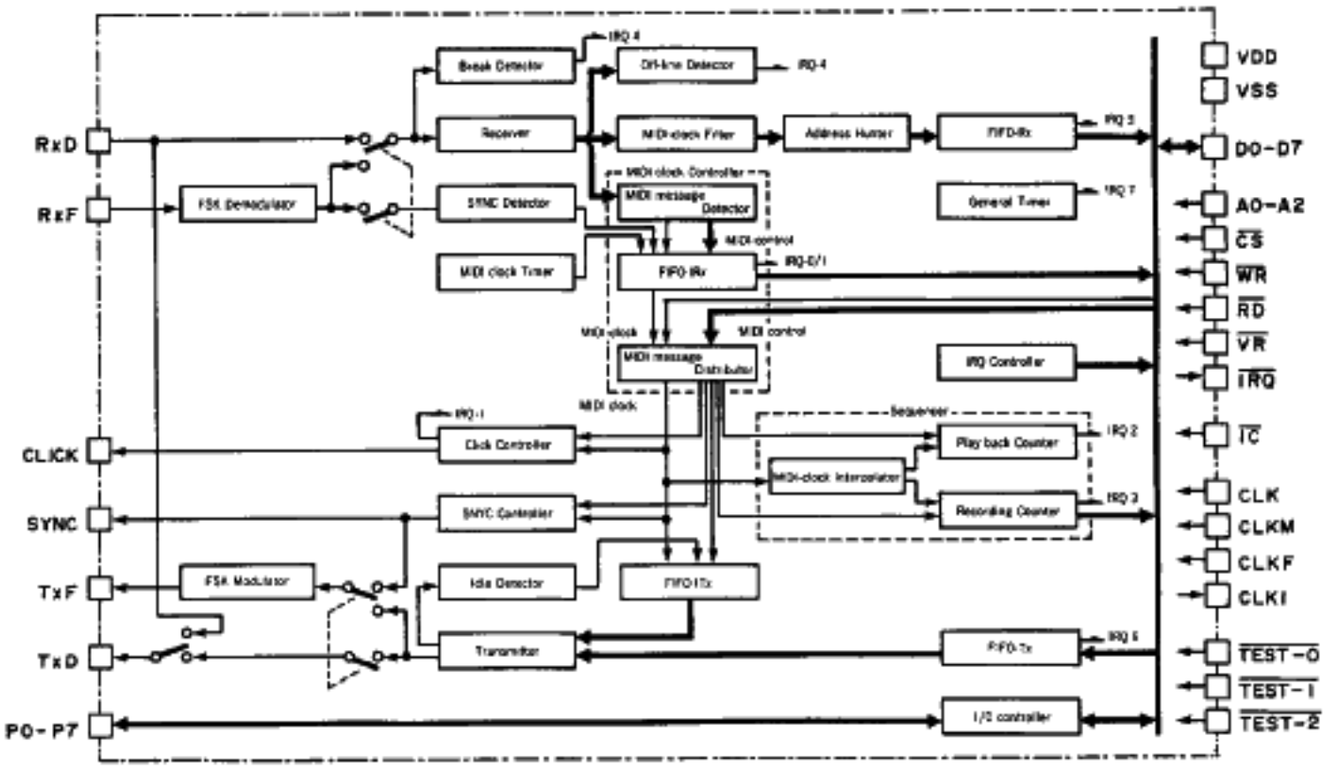
- Vector output function according to 8-level interruput factors

- C-MOS, 4MHz maximum system clock, 50mW power consumption (10mA current consumption)

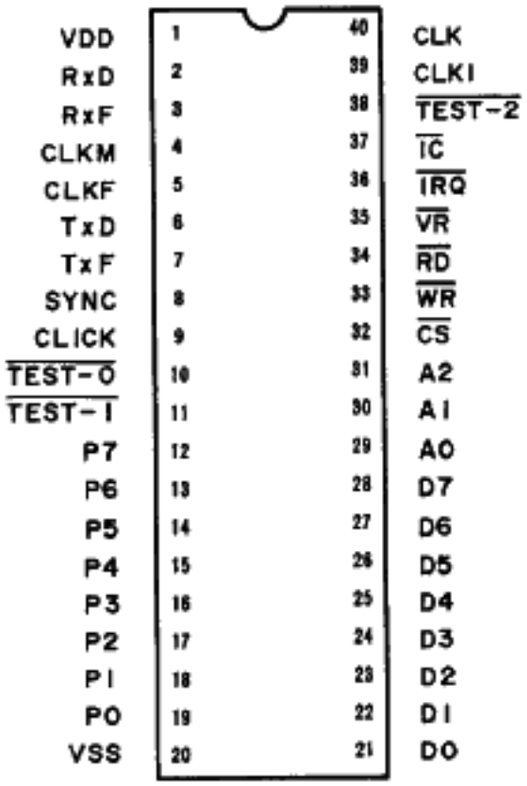
- Single 5V power supply, TTL level interface

- Package: 40-pin DIP

■ BLOCK DIAGRAM



■ PIN ASSIGNMENT



■ PIN FUNCTIONS

The pin configuration is shown in Fig. 2.1.

- $\overline{IC}$ ... Input
  The YM3802 is reset by the low level input signal to this terminal. The reset pulse width must be more than 32 clocks of the system clock to the CLK terminal (32 TCLK).
  The same reset operation can be made by the host CPU operation on the internal registers of YM3802.

- CLK ... Input
  System clock input terminal
  The internal operation of the YM3802, input signal sampling and output signal changing are all performed in synchronization with the internal timing clock made by this system clock. The clock rate must be more than 32 times the communication rate used. In the case of an MIDI communication rate of 31.25K bps at least a 1MHz clock rate is necessary. The maximum rate is 4MHz.

- CLKI ... Output
  Internal timing clock output terminal.

- CLKM ... Input
  Input terminal for a clock that generates an MIDI communication rate of 31.25K bps (baud). Usually 1MHz or 0.5MHz is input, and 1/16 or 1/32 of this can be used as the communication rate.
  This clock signal is divided to obtain a count clock for the general-purpose timer and the MIDI clock timer and also for the output pulse width at the SYNC and CLICK terminals. A divide-by-two circuit is included so that the same setting time can be obtained, irrespective of the input signal to the CLKM terminal (1MHz or 0.5MHz).

- CLKF ... Input
  Input terminal for a clock that generates a communication rate of 75×2^n series.
  Usually an input of 614.4KHz is required to obtain the communication rates from 1/8192nd of this frequency (75 bps) to 1/32nd of the same frequency (19200 bps). This input can be used also for counting in the MIDI active sense function.

- D0 ~ D7 ...Input/Output
  A0 ~ A2 ..... Input
  $\overline{CS}$ ..... Input
  $\overline{WR}$ ..... Input
  $\overline{RD}$ ..... Input
  $\overline{VR}$ ..... Input
  $\overline{IRQ}$ ..... Output
  These terminals are used to provide interface to the host CPU.

- $\overline{\text{TEST-0}}$ ~ $\overline{\text{TEST-2}}$ ... Input
  Terminals used for testing the LSI. Thus, no connections are generally made.

- RxD ... Input
  Serial data input terminal

- TxD ... Output
  Serial data output terminal

- RxF ... Input
  Audio signal input terminal from the magnetic tape such as a cassette tape. FSK-modulated serial data are input to this terminal at the TTL level.

- TxF ... Output
  Audio signal output terminal to the magnetic tape such as a cassette tape. FSK-modulated serial data are output from this terminal at the TTL level.

- SYNC ... Output
  A 2msec width pulse is output from this terminal in synchronization with the MIDI clock. It is used as a SYNC signal for other hardware.

- CLICK ... Output
  A 2msec width pulse is output from this terminal in synchronization with the MIDI clock signal. These pulses occur at a frequency that is a fraction of the MIDI clock signal frequency. It can be used as a metronome, etc., which is synchronized with the MIDI clock.

- P0 ~ P7 ... Input/Output
  General-purpose I/O port with which the input/output direction of each bit can be separately set.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNITS
Supply voltage	V_{DD}	−0.3 ~ +7.0	V
Input voltage	V_I	−0.3 ~ +0.5	V
Operating temperature	Top	0 ~ 70	°C
Storage temperature	Tstg	−50 ~ 125	°C

Recommended Operating Conditions (Ta = 0~70°C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNITS
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Top	0		70	°C

Electrical Characteristics

(A) DC characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input low level voltage	V_{IL}		−0.3	—	0.8	V
Input high level voltage	V_{IH}		2.0	—	V_{DD}+0.5	V
Input leakage current	I_{LK}	V_I = 0~5V (Except for the pins with pull-up registers)	—	—	10	μA
Pull-up resister	Ru	($\overline{TEST0}$~$\overline{TEST2}$, $\overline{IC}$)	100	—	1000	KΩ
Output low level voltage	V_{OL}	I_{OL} = 2mA ($P0$~$P7$, $D0$~$D7$, $\overline{IRQ}$)	Vss	—	0.4	V
Output low level voltage	V_{OL}	I_{OL} = 1mA (Output terminals other than shown above)	Vss	—	0.4	V
Output high level voltage	I_{OL}	I_{OH} = −1mA (Except for $\overline{IRQ}$)	4.0	—	V_{DD}	V
Output leakage current	I_{OL}	V_O = 0 ~ 5V	—	—	10	μA
Power supply current	I_{DP}	V_{DD} = 5V	—	6	10	mA
Input capacitance	C_I	f = 1MHz	—	—	10	pF
Output load capacitance	C_{L1}	$P0$~$P7$, $D0$~$D7$, $\overline{IRQ}$	—	—	100	pF
	C_{L2}	Output terminals other than shown above	—	—	50	pF

(B) AC characteristics

• CLK input

ITEM	SYMBOL	MIN.	MAX.	UNIT
CLK Cycle time	t_{CC}	250	2500	n sec
CLK H level setup time	t_{HC}	100	—	n sec
CLK L level setup time	t_{LC}	100	—	n sec
CLK Build up time	t_{RC}	—	20	n sec
CLK Release time	t_{FC}	—	20	n sec

• CLK input and output pins

ITEM	SYMBOL	MIN.	MAX.	UNIT
CLK-CLKI Delay time*1	t_{DCC}	—	50	n sec
CLK-output change over delay time*1	t_{DOC}	—	100	n sec

*1 : CLIK, SYNC, TXF, TXD, $\overline{IRQ}$

• Register write

ITEM	SYMBOL	MIN.	MAX.	UNIT
Address setup time	t_{SAW}	20	—	n sec
Address hold time	t_{HAW}	20	—	n sec
CS · WR Pulse width	t_{WW}	100	—	n sec
Data setup time	t_{SDW}	50	—	n sec
Data hold time	t_{HDW}	20	—	n sec

• Register read-out

ITEM	SYMBOL	MIN.	MAX.	UNIT
Address setup time	t_{SAR}	20	—	n sec
Address hold time	t_{HAR}	20	—	n sec
CS · WR Setup time*2	t_{SRC}	0	—	n sec
$\overline{CS}$ · $\overline{WR}$ Hold time*2	t_{HRC}	150	—	n sec
Data access time*2	t_{ADC}	—	150	n sec
Data hold time	t_{HDR}	5	—	n sec

*2 : Time corresponding to the CLK

• IRQ vector read-out

ITEM	SYMBOL	MIN.	MAX.	UNIT
$\overline{VR}$ Setup time*	t_{SVC}	0	—	n sec
$\overline{VR}$ Hold time*	t_{HVC}	150	—	n sec
Data access time*	t_{ADC}	—	150	n sec
Data hold time	t_{HDV}	5	—	n sec

* : Time corresponding to the CLK

• I/O port output

ITEM	SYMBOL	MIN.	MAX.	UNIT
Clock setup time	t_{SCW}	70	—	n sec
$\overline{CS}$ · $\overline{WR}$ Setup time	t_{SWC}	0	—	n sec
I/O port hold time	t_{APC}*	100	—	n sec

• I/O port input

ITEM	SYMBOL	MIN.	MAX.	UNIT
Clock setup time	t_{SCR}	70	—	n sec
$\overline{CS}$ · $\overline{RD}$ Setup time	t_{SRC}	0	—	n sec
I/O port setup time	t_{SPC}	0	—	n sec
I/O port hold time	t_{HPC}	100	—	n sec

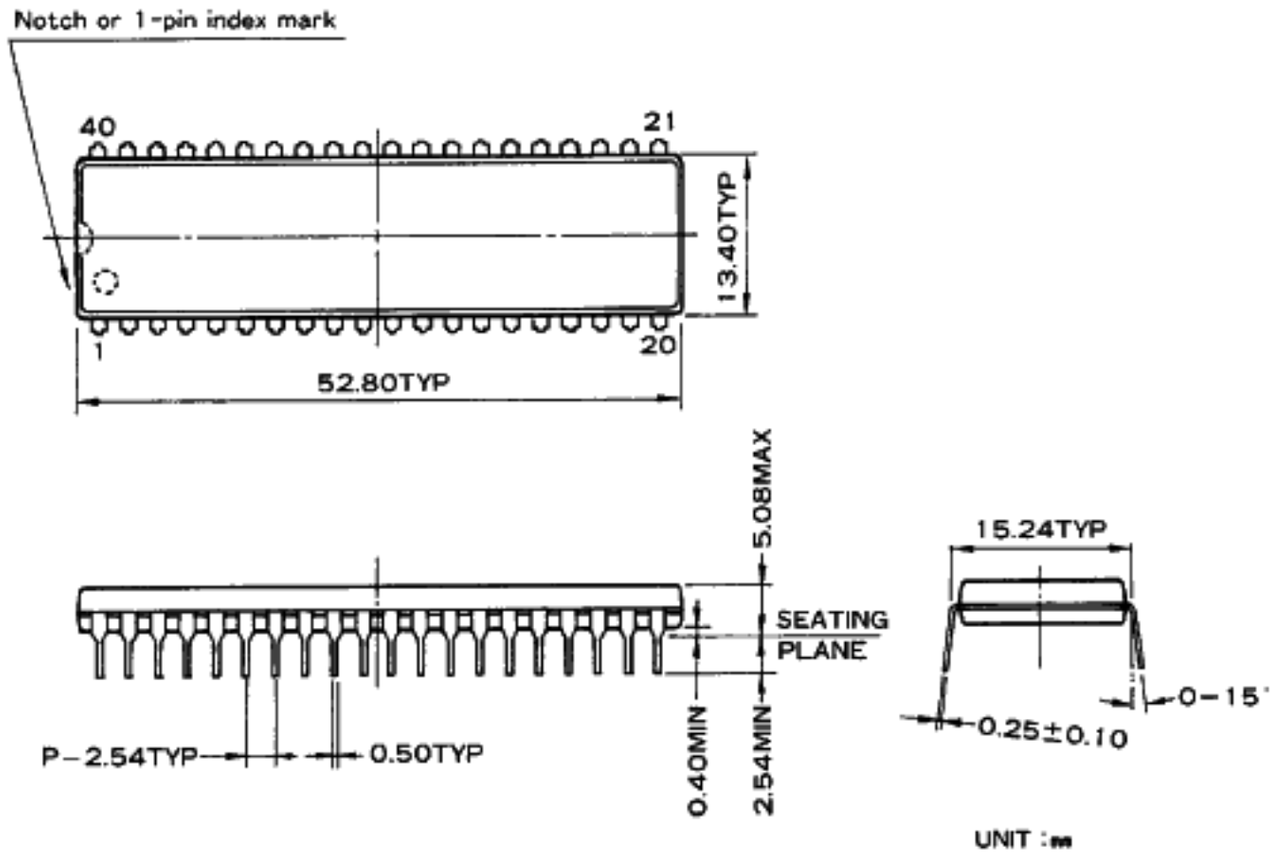
• Terminal input (CLKM, CLKF, RxD, RxF, $\overline{IC}$)

ITEM	SYMBOL	MIN.	MAX.	UNIT
Input signal setup time	t_{SIC}	0	—	n sec
Input signal hold time	t_{HIC}	70	—	n sec

(Note 1) : Perfect operation of the $\overline{IC}$ requires sampling on the L level 32 times.

(Note 2) : At least one sampling is made if the setup period for the L-or H-level is T CLK or more.

■ OUTLINE DIMENSIONS



The specifications of this product are subject to improvement changes without prior notice.

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